1. A device comprising a memory cell, wherein said memory cell comprises:

a semiconductor substrate;

a switching device disposed over said semiconductor substrate;

a charge storage device in electrical communication with said switching device;

a plurality of topographic structures comprising:

at least one first topographic structure including conductive lead lines deposited over said semiconductor substrate and in electrical communication with said switching device, said at least one first topographic structure including a top surface; and

a plurality of second topographic structures with top surfaces thereon, said top surfaces of said second topographic structures generally co-planar with said top surfaces of said at least one first topographic structure;

at least one geometrically simple array comprising at least a portion of said plurality of first and second topographic structures such that:

the periphery of said at least one geometrically simple array is substantially bounded by straight edges of said plurality of second topographic structures; and

no portion of said plurality of second topographic structures within said array extends laterally beyond said periphery;

a gridded valley disposed within said array and including an interconnected series of spaces between adjacent topographic structures, wherein:

a lateral distance defining a width of any one of said series of spaces is substantially equal to that of another of said series of spaces within said gridded valley;

the longest linear dimension of each of said series of spaces is no longer than the longest dimension of any of said second topographic structures; and

no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions; and

a planarization layer deposited over said substrate such that it is disposed at least within said gridded valley and laterally surrounds said plurality of topographic structures.

2. A device according to claim 1, wherein said width of each of said interconnected series of spaces is between 0.25 and 0.5 micron.

3. A device according to claim 1, wherein an arrangement of said plurality of second topographic structures define a first orthogonal in-plane dimension and a second orthogonal in-plane dimension.

4. A device according to claim 3, wherein at least one of said dummy fills overlaps with at least one adjacent dummy fill along at least one of said first and second in-plane dimensions.

5. A device according to claim 1, wherein said planarization layer comprises TEOS.

6. A device according to claim 1, wherein said planarization layer comprises spin-on glass.

7. A device according to claim 1, wherein said dummy fill is T-shaped.

8. A device according to claim 7, further comprising a second set of said dummy fills disposed between said T-shaped dummy fills.

9. A device according to claim 8, wherein said second set of said dummy fills are square-shaped.

10. A device according to claim 1, wherein said dummy fills are made of the same material as said conductive lead lines.

11. A device according to claim 1, wherein a first set of said interconnected series of spaces extend in a first orthogonal in-plane dimension, while said second set of said interconnected series of spaces extend in a second orthogonal in-plane dimension.

12. A device according to claim 1, further comprising a motherboard comprising:
a mount for a microprocessor;

a mount for a plurality of said memory cells;

a mount for a plurality of controller sets; and

a plurality of interconnect devices to provide electrical communication between said motherboard and said mounts.

13. A device according to claim 12, further comprising:

a microprocessor disposable on said motherboard;

at least one input electrically coupled to said microprocessor;

at least one mass storage unit electrically coupled to said microprocessor; and

at least one output electrically coupled to said microprocessor such that said motherboard, microprocessor, memory cells, input, output and mass storage unit define a computer system.

14. A memory cell comprising:

a substantially planar semiconductor substrate defining first and second orthogonal in-plane dimensions;

a switching device disposed over said semiconductor substrate;

a charge storage device in electrical communication with said switching device;

a plurality of first topographic structures comprising conductive lead lines deposited over said semiconductor substrate and in electrical communication with said switching device, said topographic structures including a top surface;

a plurality of second topographic structures with top surfaces thereon, said plurality of second topographic structures comprising the same material as said plurality of first topographic structures and defining first and second in-plane dimensions, and at least one of said fill patterns overlaps with at least one adjacent fill pattern along at least one of said first and second in-plane dimensions, wherein at least a portion of said second topographic structures are T-shaped, said top surfaces of said second topographic structures generally co-planar with said top surfaces of said plurality of first topographic structures;

at least one geometrically simple array comprising at least a portion of said plurality of first and second topographic structures arranged over said semiconductor substrate such that:

the periphery of said at least one geometrically simple array is substantially bounded by straight edges of said plurality of second topographic structures; and

no portion of said plurality of second topographic structures within said array extends laterally beyond said periphery;

a gridded valley disposed within said array, said gridded valley comprising a first set of interconnected series of spaces that extend in said first orthogonal in-plane dimension, and a second set of said interconnected series of spaces that extend in said second orthogonal in-plane dimension such that:

said first and second set of interconnected series of spaces between adjacent ones of said first and second topographic structures define a width of any one of said interconnected series of spaces between 0.25 and 0.5 micron;

the longest linear dimension of each of said interconnected series of spaces is no longer than the longest dimension of any of said second topographic structures; and

no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions; and

a TEOS planarization layer deposited over said substrate such that it is disposed at least within said gridded valley and laterally surrounds said plurality of first and second topographic structures.

15. A device comprising a memory cell, wherein said memory cell comprises:

a substrate with a plurality of peaks and valleys, where said peaks are defined by at least one topographic conductive line spaced apart from a plurality of topographic dummy patterns, and said valleys are defined by interpeak spaces that are formed between said peaks;

a switching device disposed over said semiconductor substrate;

a charge storage device in electrical communication with said switching device;

a repeating array defined by at least a portion of said plurality of peaks and valleys, wherein:

the periphery of said array is substantially bounded by straight edges of said plurality of dummy patterns; and

no portion of any of said plurality of said dummy patterns within said array extends laterally beyond said periphery of said array;

a grid disposed within said array, said grid defined by said interpeak spaces such that the longest linear dimension of each of said valleys is no longer than the longest lateral dimension of any of said dummy patterns, and no intersection defined by a crossing between any two of said interpeak spaces includes uninterrupted linear dimensions; and

a substantially planar layer of insulative material deposited over said valleys, said planar layer having a thickness selected to render a top surface of said substantially planar layer substantially co-planar with a top surface of said peaks.